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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,543	07/19/2006	Yasuhito Urashima	Q79654	6159

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EXAMINER	
AHMED, SELIM U	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/586,543	URASHIMA, YASUHITO	
	Examiner	Art Unit	
	SELIM AHMED	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *16 and 17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/19/2006, 10/4/2007, 04/30/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, including claims 1-15 in the reply filed on 02/15/2009 is acknowledged.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed on 06/05/2008.

Information Disclosure Statement

3. The Information Disclosure Statements filed on 07/19/2006, 10/04/2007 and 04/30/2008 have been considered.

Oath/Declaration

4. The oath or declaration filed on 07/19/2006 is acceptable.

Drawings

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following claimed features must be shown or the feature(s) canceled from the claim(s).

    a. An n-type layer

b. A p-type layer

c. Light emitting layer

d. A negative electrode

e. A positive electrode

No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 3, 5-10, 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sunakawa et al (US 2003/0207125; Sunakawa hereinafter) in view of Ishida (US 6,864,158: Ishida hereinafter).

With regard to claim 1, Sunakawa discloses a Group III nitride (e.g. Abstract) semiconductor multilayer structure (e.g. Figs. 1A-1F) comprising a substrate 11; an AlxGa1-xN (0≤x≤1) buffer layer 12 which is provided on the substrate 11 and has a columnar or island-like crystal structure (e.g. Fig. 1C, para[0107]); and an AlxInyGa1-x-yN (0≤x≤1, 0≤y≤1, (0≤x + y≤1) single-crystal layer 15 provided on the buffer layer 12, wherein the substrate 11 has, on its surface, non-periodically (e.g. Figs. 1C-1F show non-periodic grooves) distributed grooves 14.

As discussed above, Sunakawa discloses all of the limitations of claim 1 with the exception of the groove 14 having an average depth of 0.01 to 5 um. In para[0107] of Sunakawa discloses that groove 14 is formed during Phosphoric

acid and Sulfuric acid etch (1:1 volume ratio) of GaN layer 12 since the acid ratio also etches sapphire substrate 11. However, for example, in Fig. 1C, col.9, lines 51-57 of Ishida discloses the sapphire substrate 11 was etched to form groove 11 to a depth of 0.1 to 1 um. It would have been obvious to one of ordinary skill in the art to form the groove having an average depth of 0.01 to 5 um through routine experimentation of the etching chemistry/parameters. It is well known in the semiconductor fabrication process to optimize the etching thickness of any particular parameter within a technology using design of experiment (DOE) technique to meet certain product specific performance and reliability. Moreover, there is no evidence indicating the ranges of the height of the thickness is critical and it has been held that it is not inventive to discover the optimum or workable range of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicants must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir.1990).

With regard to claim 2, Fig. 1C, col.9, lines 51-57 of Ishida discloses a Group III nitride semiconductor multilayer structure according to claim 1, wherein the grooves have an average depth of 0.1 to 1 um.

With regard to claim 3, Sunakawa (in view of Ishida) discloses all of the limitations of claim 1, with the exception of the Group III nitride semiconductor multilayer structure wherein the substrate is formed of sapphire single crystal or SiC single crystal. Sunakawa discloses the Group III nitride semiconductor multilayer structure, wherein the substrate is formed of sapphire crystal, however. It would have been obvious to one having ordinary skill in the art at the time of the invention to use single crystal sapphire substrate for superior electrical properties.

With regard to claim 5, e.g. para[0075] of Sukanawa (in view of Ishida) discloses a Group III nitride semiconductor multilayer structure according to claim 1, wherein the buffer layer has a thickness of 1 to 100 nm.

With regard to claim 6, e.g. para[0106] of Sunakawa discloses a Group III nitride semiconductor multilayer structure according to claim wherein the buffer layer is formed through continuously feeding of a Group III element source and a nitrogen source or through feeding of merely a Group III element source (in the case where the nitrogen/Group III element ratio is zero).

Sunakawa does not disclose the ratio of nitrogen to a Group III element becomes 1,000 or less explicitly. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize the ratio of

nitrogen to a Group III element becomes 1,000 or less, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. See also In re Peterson, 65 USPQ2d 1379.

Furthermore, applicant's claim 6 does not distinguish over the Sunakawa's reference regardless of the process used to form the Group III nitride semiconductor multilayer structure because only the final product is relevant, not the process of making such as, formed through specific gas ratio. Note that a "product by process claim" is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

With regard to claim 7, Sunakawa (in view of Ishida) discloses the claimed invention except for the single-crystal layer has a thickness of 1 to 20 um.

Sunakawa discloses the single crystal layer has a thickness of 8 um or more (para[0109]). In para[0135], Sunakawa further discloses, "In order to preferably form the particulate GaN film, the thickness of the GaN film is preferably appropriately set in accordance with a temperature raising speed, growth temperature, and H2 or NH3 partial pressure". It would have been obvious to one of ordinary skill in the art at the time the invention was made to grow 1 to 20 um of single crystal, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. See also In re Peterson, 65 USPQ2d 1379.

With regard to claim 8, e.g. para[0108] of Sunakawa discloses A Group III nitride semiconductor multilayer structure according to claim 1 wherein the single-crystal layer is formed through feeding of a Group III element source and a nitrogen source.

As discussed above, Sunakawa does not disclose the nitrogen/Group III element ratio becomes 1,600 to 3,200. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize the nitrogen/Group III element ratio from 1,600 to 3,200 since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering

the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. See also In re Peterson, 65 USPQ2d 1379.

Furthermore, applicant's claim 8 does not distinguish over the Sunakawa's reference regardless of the process used to form the Group III nitride semiconductor multilayer structure because only the final product is relevant, not the process of making such as, formed through specific gas ratio. Note that a "product by process claim" is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

With regard to claim 9, Sunakawa does not disclose a Group III nitride semiconductor multilayer structure according to claim 1 wherein the single-crystal layer is formed while the temperature of the substrate is regulated so as to fall

within a range of 1,000 to 1,300°C. Sunakawa discloses the temperature range from 600C to 1040C (para[0108]) rather. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize the temperature of the substrate is regulated so as to fall within a range of 1,000 to 1,300°C since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. See also In re Peterson, 65 USPQ2d 1379.

Furthermore, applicant's claim 9 does not distinguish over the Sunakawa's reference regardless of the process used to form the Group III nitride semiconductor multilayer structure because only the final product is relevant, not the process of making such as, formed through specific temperature. Note that a "product by process claim" is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not.

Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

With regard to claim 10, Sunakawa (in view of Ishida) discloses the claimed invention except for the temperature of the substrate regulated so as to fall within a range of 1,050 to 1,200°C. It would have been obvious to one of ordinary skill in the art at the time the invention was made to regulate the temperature within 1,050 to 1,200°C, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. See also In re Peterson, 65 USPQ2d 1379.

With regard to claim 13, Sunakawa discloses a substrate 11 for forming a Group III nitride semiconductor, which has, on its surface, non- periodically (e.g. Figs. 1C-1F show non-periodic grooves) distributed grooves 12.

As discussed above, Sunakawa discloses all of the limitations of claim 13 with the exception of the groove 14 having an average depth of 0.01 to 5 um. In para[0107] of Sunakawa discloses that groove 14 is formed during Phosphoric acid and Sulfuric acid etch (1:1 volume ratio) of GaN layer 12 since the acid ratio also etches sapphire substrate 11. However, for example, in Fig. 1C, col.9, lines 51-57 of Ishida discloses the Sapphire substrate 11 was etched to form groove

11 to a depth of 0.1 to 5 um. It would have been obvious to one of ordinary skill in the art to form the groove having an average depth of 0.01 to 5 um through routine experimentation of the etching chemistry/parameters. It is well known in the semiconductor fabrication process to optimize the etching thickness of any particular parameter within a technology using design of experiment (DOE) technique to meet certain product specific performance and reliability. Moreover, there is no evidence indicating the ranges of the height of the thickness is critical and it has been held that it is not inventive to discover the optimum or workable range of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicants must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir.1990).

With regard to claim 14, Fig. 1C, col.9, lines 51-57 of Ishida discloses a a substrate for forming a Group III nitride semiconductor according to claim 13, wherein the grooves have an average depth of 0.1 to 1 um.

With regard to claim 15, Sunakawa (in view of Ishida) discloses all of the limitations of claim 13 respectively, with the exception of the Group III nitride

semiconductor multilayer structure wherein the substrate is formed of sapphire single crystal or SiC single crystal. Sunakawa discloses the Group III nitride semiconductor multilayer structure, wherein the substrate is formed of sapphire crystal, however. It would have been obvious to one having ordinary skill in the art at the time of the invention to use single crystal sapphire substrate for superior electrical properties.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sunakawa in view of Cuomo et al (US 2002/0078881; Cuomo hereinafter).

With regard to claim 4, Sunakawa discloses all of the limitations of claim 1 with the exception of a Group III nitride semiconductor multilayer structure according to claim 1, wherein the buffer layer contains columnar crystal grains. However, e.g. Fig. 4, element 14, para[00041] of Cuomo discloses a buffer layer with columnar crystal grains. Para [00041] of Cuomo discloses, “It is another object of the present invention to provide such columnar structures as strain-relieving buffer or transition layers or seed crystals for the growth of additional low-defect density Group III materials thereon.” It would have been obvious to one having ordinary skill in the art at the time of the invention to include columnar structure buffer layer such as taught by Cuomo et al. within Sunakawa’s device for predictable results.

8. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sunakawa in view of Uemura et al (US 6,917,059; Uemura hereinafter).

With regard to claim 11, Sunakawa discloses all of the limitations of claim 1 with the exception of a Group III nitride semiconductor light-emitting device comprising a Group III nitride semiconductor multilayer structure according to claim 1; Group III nitride semiconductor layers provided atop the single-crystal layer of the semiconductor multilayer structure, the semiconductor layers including an n-type layer, a light-emitting layer, and a p-type layer; and a negative electrode and a positive electrode which are provided at predetermined positions. However, Fig. 2 of Uemura discloses a Group III nitride semiconductor light-emitting device (Fig. 2) comprising a Group III nitride semiconductor (Abstract) multilayer structure according to claim 1; Group III nitride semiconductor layers 23, 24, 25 (col.6, lines 46-50 disclosed that 23 may have a double layer structure) provided atop the single-crystal layer 23 of the semiconductor multilayer structure, the semiconductor layers including an n-type layer 23, a light-emitting layer 24, and a p-type layer 25; and a negative electrode 26 and a positive electrode 28 which are provided at predetermined positions. It would have been obvious to one having ordinary skill in the art at the time of the invention to include Uemura's an n-type layer 23, a light-emitting layer 24, and a p-type layer 25; and a negative electrode 26 and a positive electrode 28 at a predetermined position to form a LED structure.

With regard to claim 12, e.g. Fig. 2 of Uemura discloses a Group III nitride semiconductor light-emitting device according to claim 11, wherein the n-type layer 23, the light-emitting layer 24, and the p-type layer 25, which constitute the Group III nitride semiconductor layers, are successively provided atop the single-crystal layer in this order (col.6, lines 46-50 disclosed that 23 may have a double layer structure); the negative electrode 26 is provided on the n-type layer 23; and the positive electrode 28 is provided on the p-type layer 25.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELIM AHMED whose telephone number is (571)270-5025. The examiner can normally be reached on 9:00 AM-6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571)272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SA

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